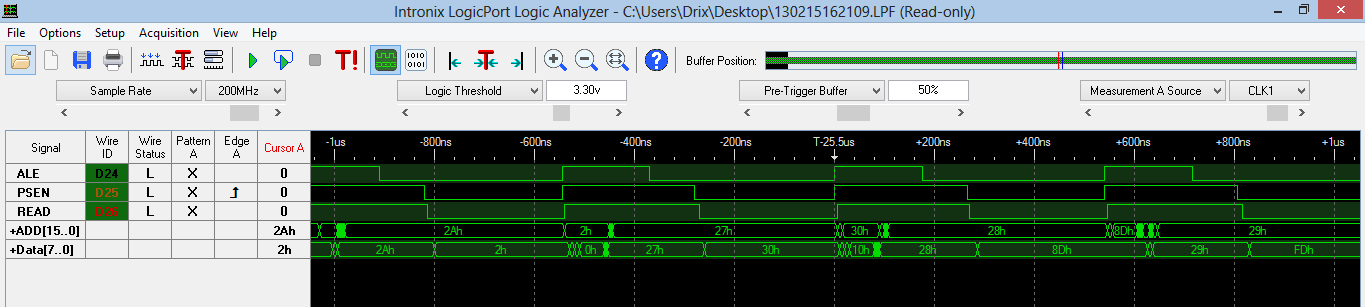
**LAB 2 REPORT**



Above shown is the logic analyzer Screen for the below code running on the microcontroller from the NVRAM:

LogDUNFIELD 8051 ASSEMBLER: SOS PAGE: 1

0000 1 ORG $0000

0000 02 00 15 2 LJMP MAIN

0015 3 ORG $0015

0015 C2 97 4 MAIN CLR P1.7

0017 74 0A 5 MOV A,#0AH

0019 75 89 01 6 MOV TMOD,#01H

001C 75 8A 00 7 BACK MOV TL0,#00H

001F 75 8C 00 8 MOV TH0,#00H

0022 D2 8C 9 SETB TCON.4

0024 30 8D FD 10 JNB TCON.5,$ >> Progression of the Data and Address in the waveform can be seen for the highlighted line

0027 B2 97 11 CPL P1.7

0029 14 12 DEC A

002A 70 F0 13 JNZ BACK

002C 79 03 14 MOV R1,#03

002E 80 01 15 SJMP D3

0030 C9 16 D2 XCH A,R1

0031 74 14 17 D3 MOV A,#14H

0033 75 8A 00 18 D1 MOV TL0,#00H

0036 75 8C 00 19 MOV TH0,#00H

0039 D2 8C 20 SETB TCON.4

003B 30 8D FD 21 JNB TCON.5,$

003E 14 22 DEC A

003F 70 F2 23 JNZ D1

0041 B2 97 24 CPL P1.7

0043 74 0A 25 MOV A,#0AH

0045 75 8A 00 26 D4 MOV TL0,#00H

0048 75 8C 00 27 MOV TH0,#00H

004B D2 8C 28 SETB TCON.4

004D 30 8D FD 29 JNB TCON.5,$

0050 14 30 DEC A

0051 70 F2 31 JNZ D4

0053 C9 32 XCH A,R1

0054 14 33 DEC A

0055 70 D9 34 JNZ D2

0057 02 00 15 35 LJMP MAIN

005A 36 ic Analyzer Screen

* The latched address still has components of the data bus when the ALE signal is high because the ‘373 is in transparent mode during this period and hence the data is still visible at the ‘373 latch output

The State Mode:

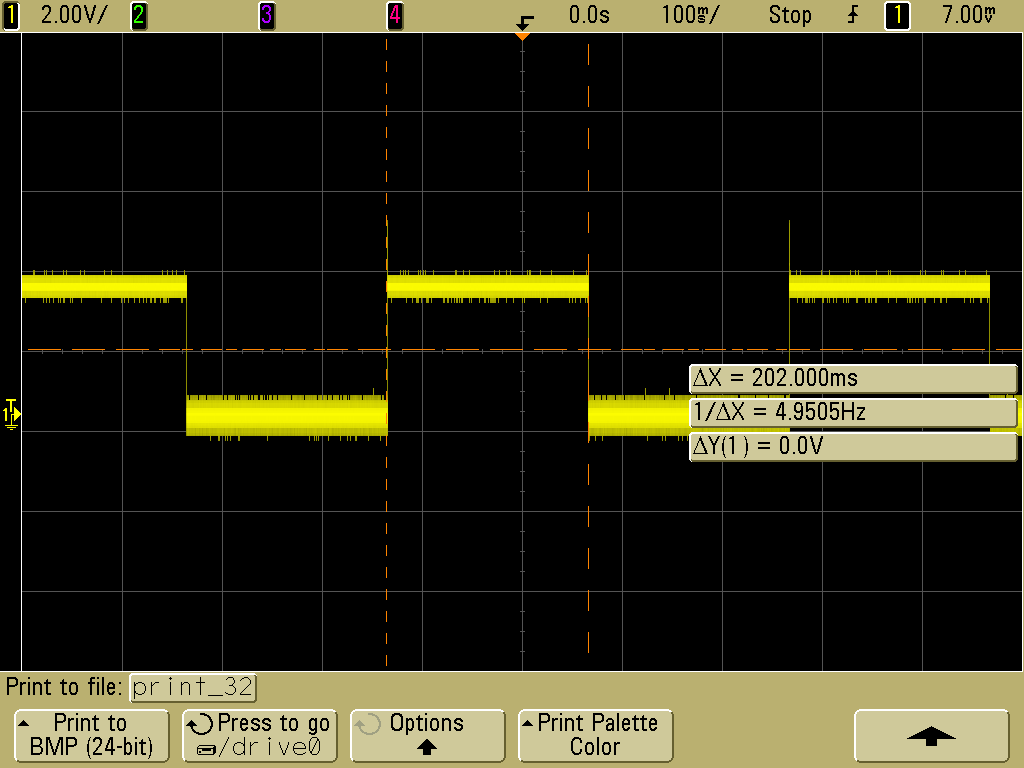
The state mode requires CLK from the external system and triggering can be used to get optimal results. From the Sample Mode in the “Logicport” analyzer a Qualifier clock can also be setup to obtain states when 2 conditions are met for acquisition.

The state mode is advantageous where there is a memory constraint for storing the capture data.

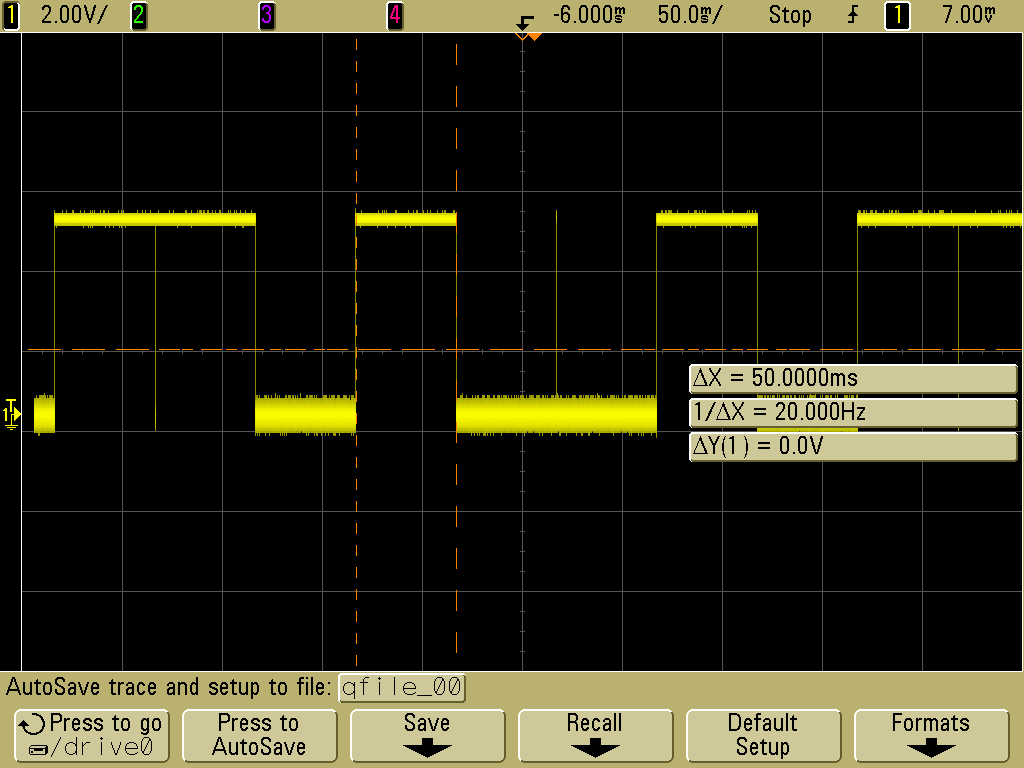
**The Toggle two pins program:**

Output of the Port pin 1.7 to be toggled at 200ms in the ISR (TJTOGGLE.LST in asm folder)

**Waveform :**



Also the ISR program that would toggle port pin 1.0 waveform is as below:



**Setup And Hold Timing Analysis:**

Setup and hold timing from the datasheet for the latch IC 74LS374 is as below:





****

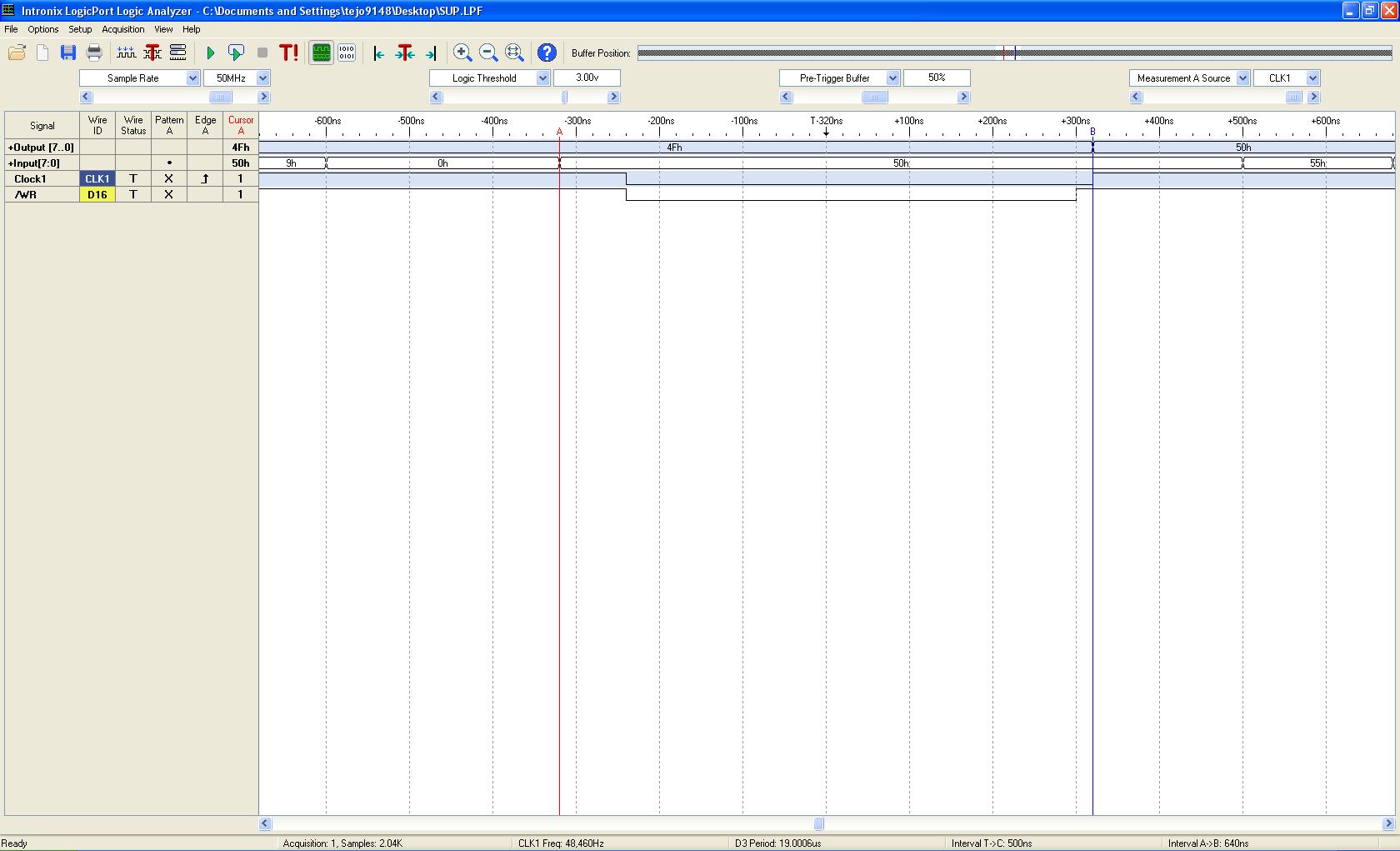
Setup Time : 20ns

Hold Time = 0ns

Propagation Delay : N.A.

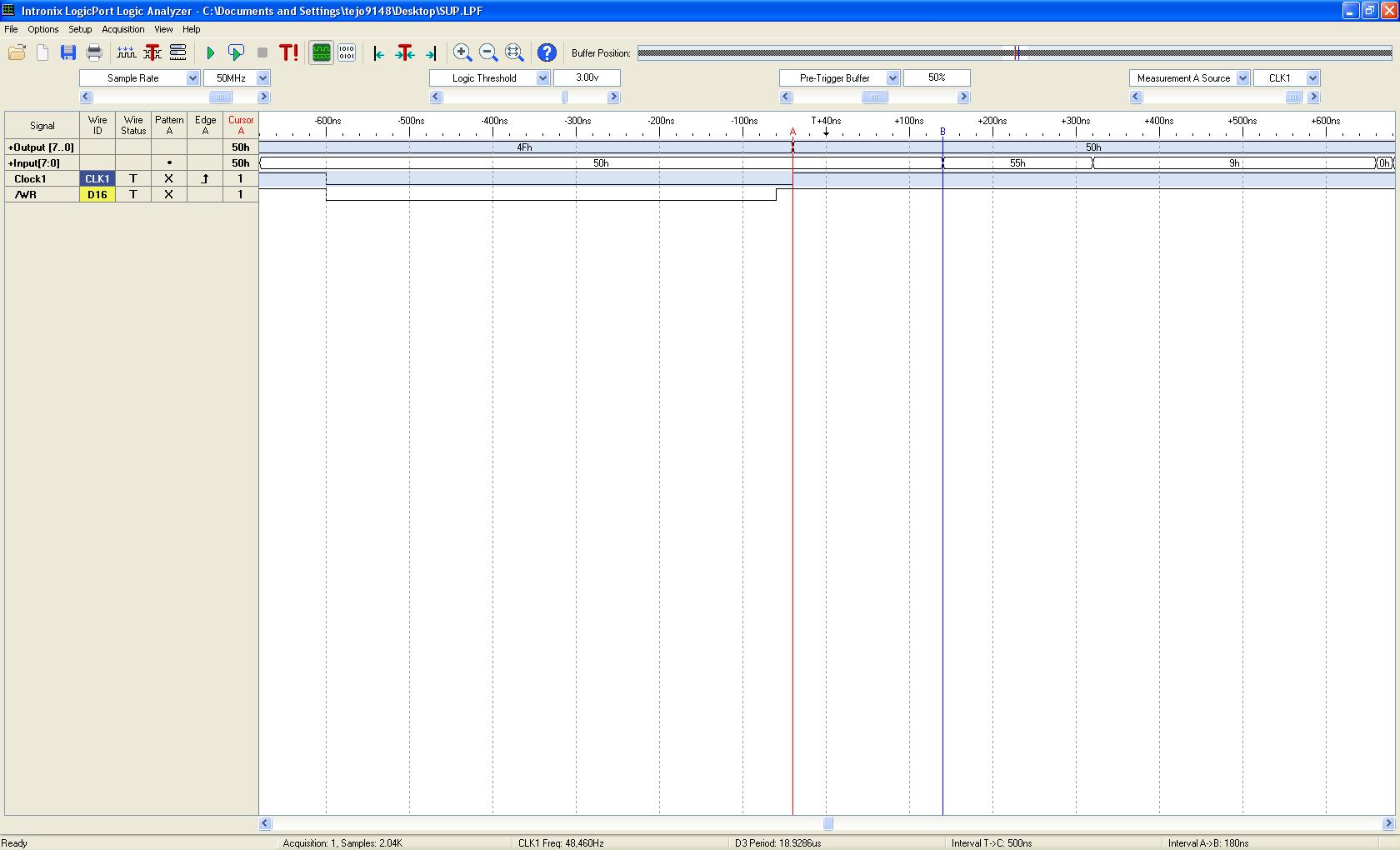
**Practical Timings with waveforms:**

Setup Time: 640ns



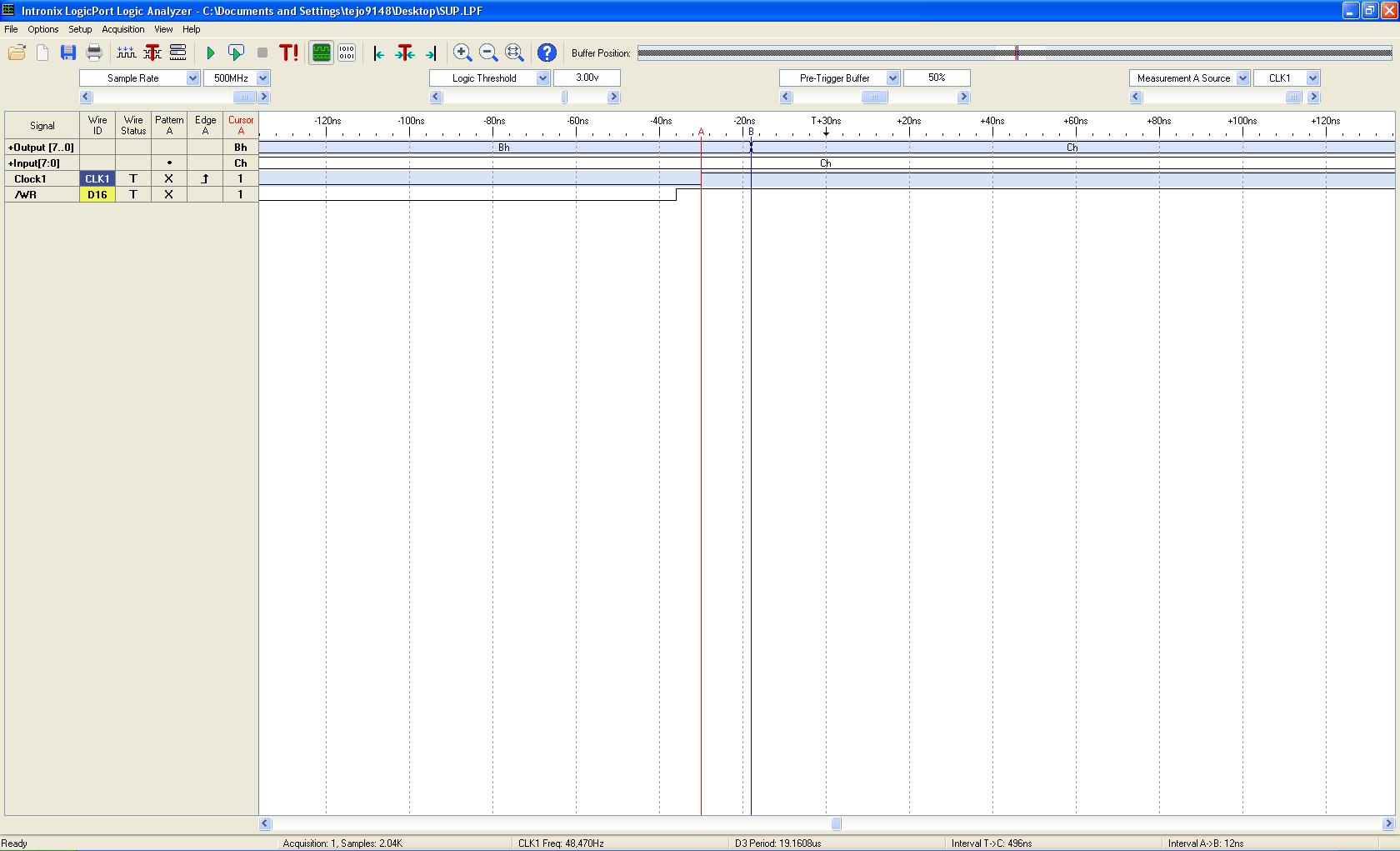
(screenshot attached : Setup Time (ts) 640ns.jpg

Hold Time: 180ns



(screenshot attached : Hold Time (th) 180ns.jpg)

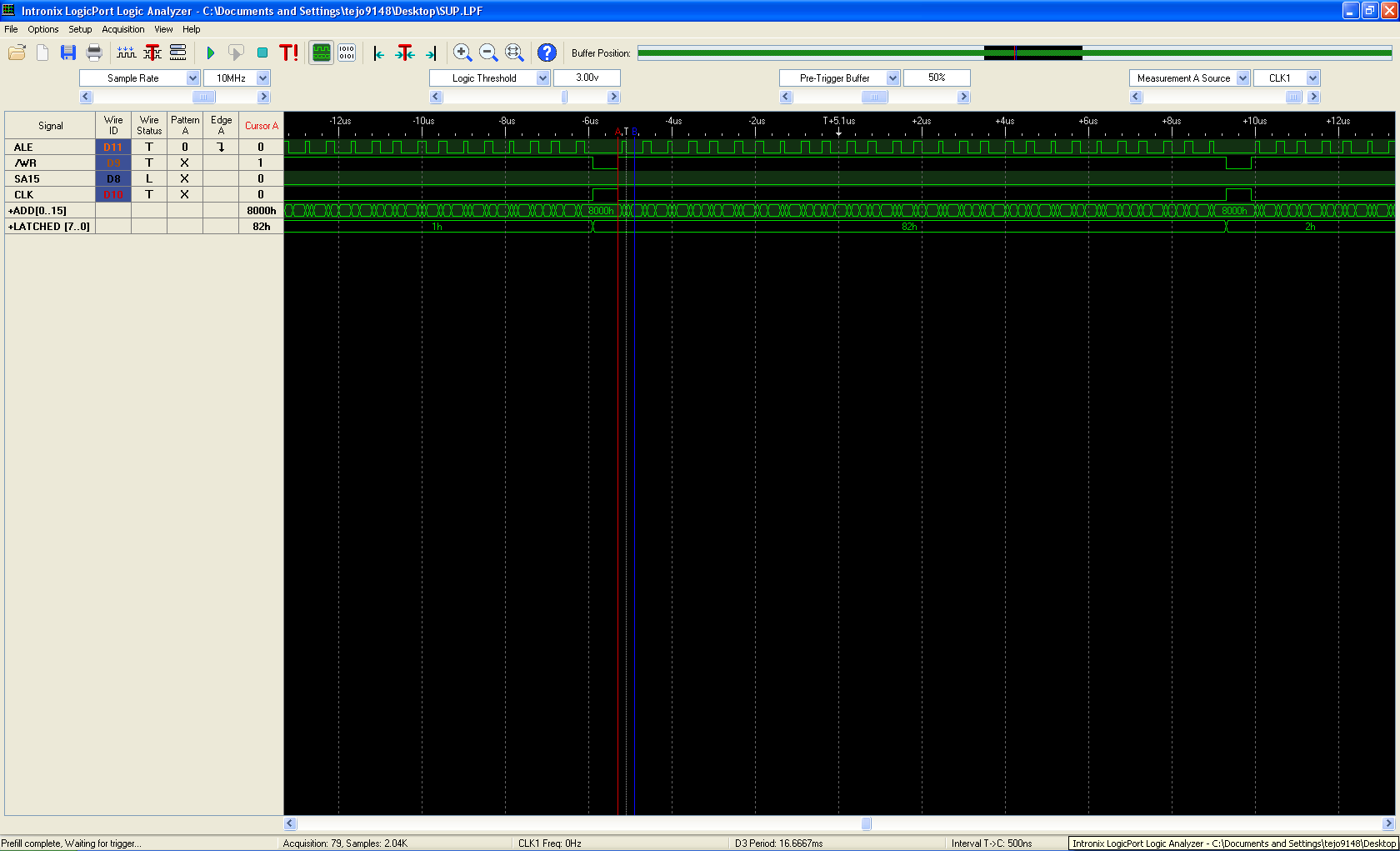
Propagation Delay:12ns



(screenshot attached : Propagation Delay (tplh) 12ns.jpg)

From the above analysis it is easy to say that the practical values satisfy the Setup and Hold Requirements in the data sheet.

Latched Data:



Above shown waveform shows the latched data at the output of latch 74374’

Progression of the latch values is as per the program TJSUP.LST(attached) which increments two loop counts one In the main program and the other in ISR.

The wave shows the progression of latch data from 1h ->82h->2h.

**The CLK signal Generation for IC 74374:**

Since we do not want the latch to be performing any operation during the address from 8000h to FFFFh we use A15 along with WR(bar) signal for generation of the CLK /CP signal for the latch.

Pin no 4 is used as WR(bar) input of the PLD and A15 is already available on pin no 6 as input to the ATF16V8C PLD ic.

The CLK signal is available at Pin no 14 being generated by the following logic:

CLK => (!A15 & WR\_AL)

The waveform at the output of pin14 is as shown below:

